Composite clock including
a Cs clock, a H-maser and a VCO

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1 Abstract

We present the project of a composite clock, that will combine a cesium standard, a hydrogen maser standard, and a voltage controlled oscillator in order to provide an output signal that would combine the respective quality of each of the component clocks, the long-term stability for the Cs clock, the mid-term stability for the H-maser and the the short-term performance for the VCO.
The output signal is provided by the VCO. Design, advances in its realizations and alternative ways that have been considered concerning its different parts are presented.
The objective is a relative frequency instability around 10^{-15} *over 1s.*

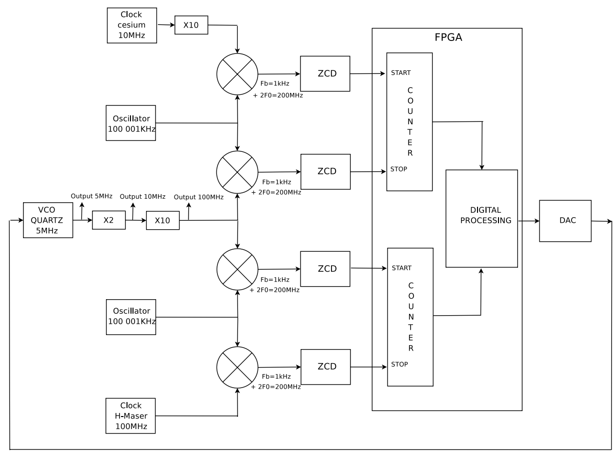

Figure 1: General diagram.

2 Introduction

The system is realized with 2 dual mixer time difference (DMTD) [1, 2]. The first allows the comparison between the CS clock and the VCO with a shifted oscillator and the second allows the comparison between H-maser clock and the VCO with the same shifted oscillator. The Figure 1 presents the whole system. The signals coming from the DMTD are send to counters realized with the help of FPGA. The signal is than treated digitally, an algorithm realizes a servoing which permits the correction of the VCO. A digital analog converter will be necessary to control the VCO in a precise way.

The whole system will function at 100 MHz which imposes the presence of many frequency multipliers, in fact only the frequency H-maser clock is at 100 MHz, the frequency of the CS clock is of 10 MHz that's why there is a multiplier by 10, that of the VCO is 5 MHz. We wish to have three outputs, one at 5 MHz, one at 10 MHz and one at 100 MHz which explains the multiplier by 2 and the multiplier by 10. The frequency of the shifted oscillator is of 100 001 KHz so that at the signal of the mixers output it's composed of a beat frequency of 1 KHz.

3 Dual Mixer Time Difference (DMTD)

The signals arriving on each mixer is a signal at 100 MHz and a signal at 100 001 Khz. The signal obtained from the output of the mixer is the following:

$$V1cos(\omega_1 t + \phi(t)) \times V2cos(\omega_2 t) \tag{1}$$

where $\omega_1 = 2\pi f1$ with the shifted frequency (f1) is at 100 001 KHz, and $\omega_2 = 2\pi f2$ whith frequency (f2) is at 100MHz comming to the Cs clock, H-Maser clock or VCO, however ω_1=ω_2+Δ_ω with $\Delta_\omega = 2\pi f_b$ with $f_b = 1KHz$. We obtain:

$$V1cos(\omega_2 t + \Delta_\omega t + \phi(t)) \times V2cos(\omega_2 t) \tag{2}$$

$$= \frac{V1V2}{2}[cos(2\omega_2 t+\Delta_\omega t+\phi(t))+cos(\Delta_\omega t+\phi(t))] \tag{3}$$

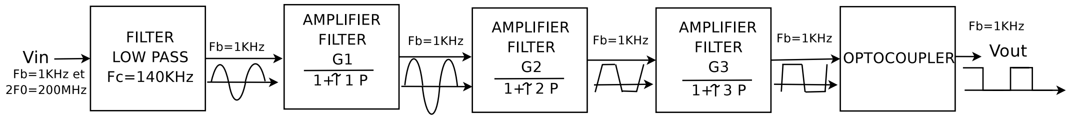

Figure 2: ZCD diagram.

We obtain a signal constituted of two components: one at 200 MHz and the other at 1 KHz. This signal enters on a Zero crossing detectors (ZCD). Each ZDC is composed of 5 stages (Figure 2) [3,4]. Each ZCD transform the sine signal of 1 KHz in an square signal of 1 Khz with a very sharp rising edge, and minima noise. The first stage of ZCD allows to delete the component at 200 MHz from the signal issued from the mixer with a low pass filter. The three stages after the first one are composed of a low pass filter with a high gain. To generate a lower noise as possible is advised to respect the following conditions for each amplification stage:

$$B_i < B_1 \Pi_{n=1}^{i-1} G_n^2 \tag{4}$$

$$G_i < \frac{2\pi B_i V_{max}}{S \Pi_{n=1}^{i-1} G_n} \tag{5}$$

Where B_i is the filter bandwidth, G_n the filter gain (dimensionless), V_{max} the maximum output voltage (V), S is the slope of the imput signal (V/s).
Diodes are placed in the feedback loop, to avoid the amplier saturation. The best compromise is to be found between higher gain, that sharpens the rising edge, and lower bandwidth that lowers noise.The last stage is composed with an optocoupler eliminating grounding issues.
For testing the ZCD, we send the same signal in two ZCD and we measure the time difference between the rising edge of two ZCD. We observed that the ZCD generated white frequency noise. The jitter measured is at about 50ns peak to peak, with a standard deviation $\sigma = 8.5ns$ (Figure 3).

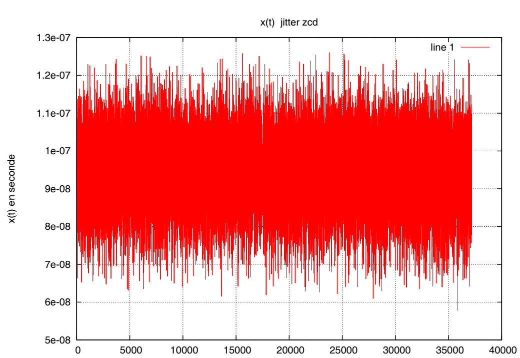

Figure 3: jitter ZCD.

Realizing a measure with an modified Allan modified deviation (Figure 4) we can decrease the uncertainty of measurement.
We will measure the beat frequency with a gate of 1s which we shift all 1ms, thus we realise a means of 1000 period in order to decrease the measure error.

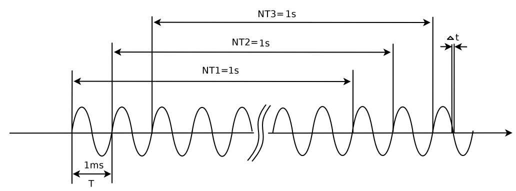

Figure 4: principle of Allan modified deviation.

We obtain the following result:

$$\sigma = 8.5ns \rightarrow 2\sigma\sqrt{2} = 24ns = \Delta t \tag{6}$$

we multiply σ by 2 because Δt corresponds at 2σ and also by $\sqrt{2}$ because there are an error at the beginning and another at the end of the gate and they are decorelated.

$$\frac{\Delta t}{NT} = \frac{24 \times 10^{(-9)}}{1} = 24 \times 10^{-9} \tag{7}$$

NT is the gate duration.

$$\frac{\Delta t}{\sqrt{1000}} = \Delta tn = 7.6 \times 10^{-10} \tag{8}$$

we divide by $\sqrt{1000}$ because there are 1000 cycles during the gate. So we spreadΔt over the 1000 cycles.

$$\frac{1}{1000} \Sigma_{i=1}^{i=1000} NT_i = < NT >^{+}_{-} \Delta tn \tag{9}$$

$$\frac{\Delta tn}{< NT >} = 7.6 \times 10^{-10} \tag{10}$$

$$\frac{100MHz}{1KHz} = 10^5 \rightarrow mod\sigma_y(1s) = \frac{7.6 \times 10^{-10}}{2 \times 10^5} \tag{11}$$

We divide by the ratio between the frequency of the system (100MHz) and the beat frequency (1KHz).

$$mod\sigma_y(1s) = 3.8 \times 10^{-15} \tag{12}$$

We obtain a σ modified Allan modified deviation at 1s that is 3.8×10^{-15}. We can increase the duration of gate, but the data will be more correleted and the correction of VCO slower. So with the system we have a relative instability at 1s lower than 4×10^{-15} at 1 σ

4 The FPGA

The FPGA has two objective: to realise the counters and the digital proccessing for the servoing of the system.

4.1 The counters

The counter is constituted in the following way: The counter of 32 bits counts permanently and at each rising edge on the start or the stop the value of the counter is stocked. These values are used to realize the servoing.

The frequency clock of counter is 100MHz, it allows to count during about 43 secondes before that the counter pass again by zero. We obtain a flexibility for the gate duration but the memory space must be sufficient. With a frequency clock of 100MHz, the measure error is $\pm 5ns$. For decrease this error we can increase the frequency clock but the gate duration should be decrease or we will raise the number of bit of the counter and the memory space.

4.2 Simulation of digital processing

In this part, we are going to simulate the servoing of the Maser clock on a cesium clock by the mean of a VCO and a quartz oscillator.
For that we note 4 steps:

1. Simulate the various noises present in the Cs clock and H-Maser clocks, the Quartz Oscillator and the Voltage control oscillator (VCO).
We know that the PSD of any oscillator could be modelled by the sum of five types noises according to this equation:

$$S_y(f) = \Sigma_{i=-2}^{i=2} h_i f^i \tag{13}$$

So, we have just to enter the values of the coefficients (h_i) in our program "bruiteur" and it will generate a sequence of frequential or temporal variation. We take 100000 samples with a step sampling is tau=100s for studying the long-term stability. We process that because we can't generate over than 2×10^6samples and for optimizing the time of our treatement.

2. Make the inter-comparison between Cs and H-Maser clocks using the VCO and the Quartz Oscillator figure(5).
a. Using a VCO having a good stability, we determinate the comparisons $(Cs - VCO)$ and $(HM - VCO)$
b. We determine the inter-comparison between Cs and H-Maser clocks $(Cs - HM)$
c. $(Cs - HM)$ passes through a digital low-pass filter whose adequate cut-off frequency (f_c) is determinated by the crossing between the DSP's curves of the Cs and H-Maser clocks see figure(6). So we have the estimated (HM_{est}).
d. This equation permits us to find $(VCO_{est}) = (HM_{est}) - (HM - VCO)$.
e. Finally we have the corrected VCO:
$VCO_{corr}(t + \tau) = VCO(t + \tau) - VCO_{est}(t)$
Remark
At first we meant to use the DMTD system with only the VCO like a common oscillator, but we risk to have the problem of a dirty signal of the Cs-clock in the short-term. Hence the DMTD can't correct the VCO. So we have decided to use a quartz oscillator with a rather good stability.

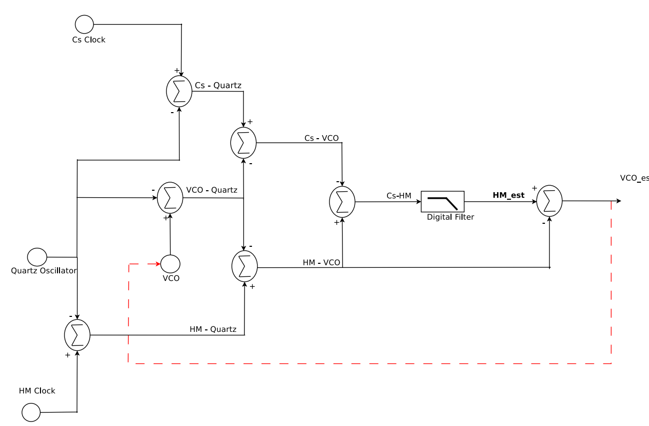

Figure 5: principle of servoing.

3. Corrections to be applied on the VCO.

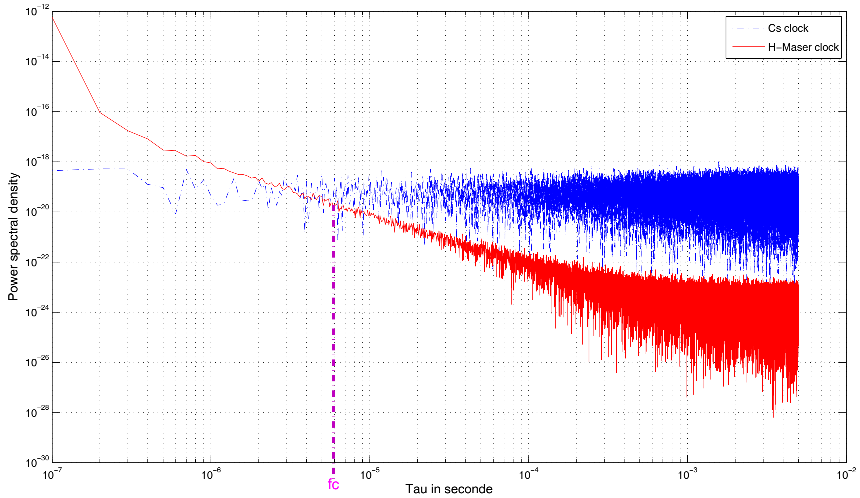

Figure 6: power spectral density of simulated cesium and maser clocks.

To summarize we have determinate at this step the corrections of the Cs and H-Maser clocks and of the VCO. Now we adjust the VCO following this equation:

$$VCO_{corr}(t+\tau) = VCO(t+\tau) - VCO_{est}(t) \quad (14)$$

with i=1....N, N=number of samples and j an integer.

4. Servoing equation.

Note that kf is the sensibility of the VCO and g(t) is the transfert function of the filter.
At the output at the VCO, we have in time domain the equation :

$$vco_{serv}(t) = vco(t) + k_f \int vco_{est}(t)dt] \quad (15)$$

And following figure(5) we determinate.
$$vco_{est}(t) = [hm(t) - cs(t)]g(t) - [hm(t) - vco(t)] \quad (16)$$

The Laplace transform applied on (15) and (16) gives

$$VCO_{serv}(p) = VCO(p) + \frac{k_f}{p}[VCO_{est}(p)] \quad (17)$$

$$VCO_{est}(p) = [HM(p) - Cs(p)]G(p) - [HM(p) - VCO(p)] \quad (18)$$

And replacing (18) in (17), we obtain :

$$VCO_{serv}(p) = VCO(p) + \frac{k_f}{p}[(HM(p) - Cs(p))G(p) - HM(p) + VCO(p)] \quad (19)$$

Now we use the Z transform posing $p = \frac{z-1}{z+1}$ for having :

$$VCO_{serv}(z) = VCO(z) + k_f \frac{z-1}{z+1} \times [(HM(p) - Cs(p))G(p) - (HM(p) - VCO(p))] \quad (20)$$

And finally using the adjusted clocks and knowing that$(z^{-1})(X(z)) = X(i-1)$ and $X(Z) = X(i)$, we find our servoing equation :

$$VCO_{serv}(i) = [\frac{1+2\pi f_c}{1+kf+2\pi f_c k_f} VCO_{corr}(i)] - [\frac{2}{1+k_f+2\pi f_c k_f} VCO_{corr}(i-1)] + [\frac{1-2\pi f_c}{1+k_f+2\pi f_c k_f} VCO_{corr}(i-2)]$$
$$+ [\frac{k_f}{1+k_f+2\pi f_c k_f} Cs_{corr}(i)] - [\frac{k_f}{1+k_f+2\pi f_c k_f} Cs_{corr}(i-2)] + [\frac{k_f 2\pi f_c}{1+k_f+2\pi f_c k_f}(HM_{corr}(i)$$
$$+2HM_{corr}(i-1) + HM_{corr}(i-2))] + [\frac{2-4\pi f_c k_f}{1+k_f+2\pi f_c k_f} + \frac{2\pi f_c + k_f - k_f 2\pi f_c - 1}{1+k_f+2\pi f_c k_f}] VCO_{serv}(i-1) \quad (21)$$

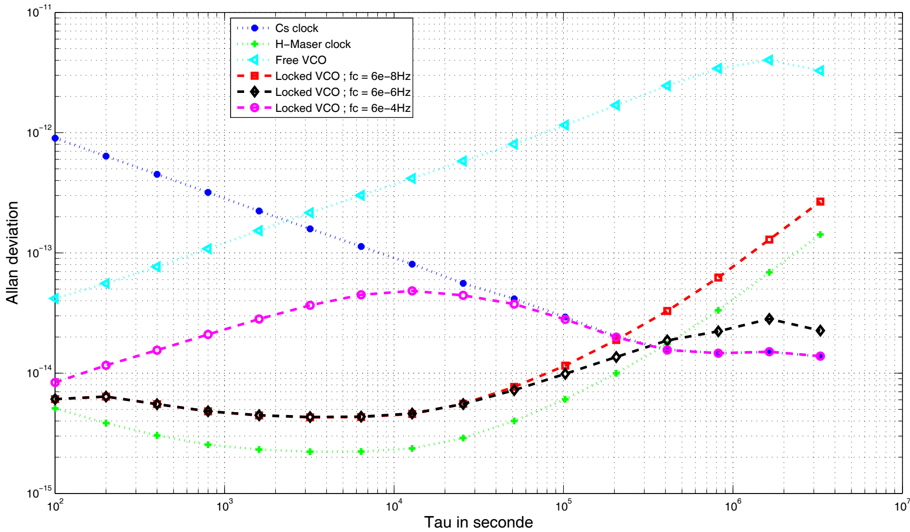

Figure 7: Effect of f_c on the stablity of the locked VCO

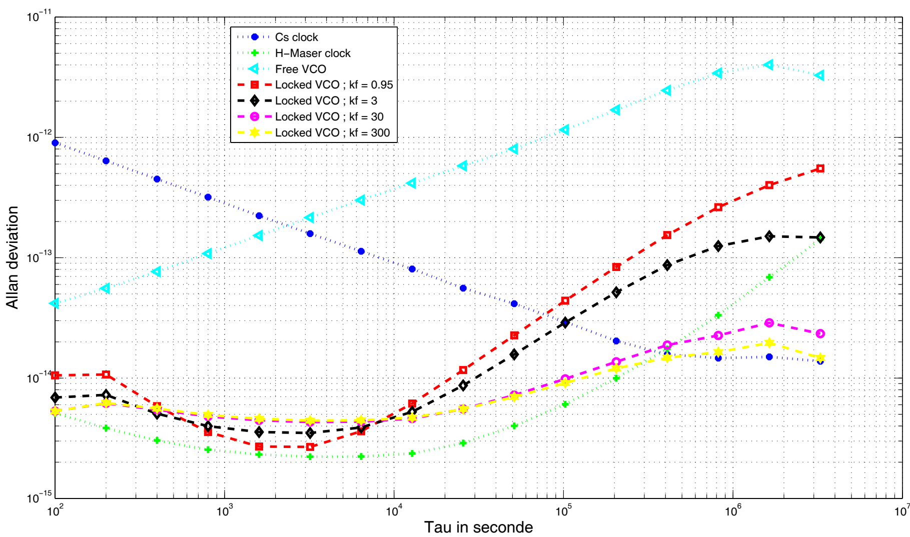

Figure 8: Effect of k_f on the stablity of the locked VCO

Simulation results and interpretations

We determine the Allan deviation of VCO_{ser} to studie the stability of the control VCO, The results of our simulation is presented in the following figures(7,8)

Results show that the stability of the control VCO depend on the cut off frequency (f_c) and on the sensitivity of the VCO. Indeed at f_c (black curve in figure (7)), that the VCO is locked in first on the H-Maser clock and then on the Cs clock. When $f_c < 6.10^{-6}$ the VCO seems to lock on the H-Maser clock (red curve) and when $f_c = 6.10^{-4}$ (magenta curve) the VCO try to be locked on the two clocks at the same time. Figure (8) highlights the influence of the VCO sensitivity k_f on the stability of the locked VCO, we note a good servoing for $k_f > 30$.

5 Conclusion

Improving the system requires increasing the slope and the stability of the ZCD. Increasing clock frequency of the counter would also directly improve its resolution. The algorithm will be modified to

find the better possible servoing.
Moreover there are other criticals elements, like the digital analog converter which controls the VCO and also the thermal drift. In fact the control voltage must be very precise i.e. the converter must have arround twenty bits, and of course the reference input voltage must be very stable. Concerning the thermal drift it must not have effect on the system. For exemple the noise of ZCD is different in fonction of temperature.

References

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